

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A chip-size semiconductor package, comprising:

- a semiconductor chip;
- a metal pad formed on the semiconductor chip;
- ~~a wafer coat formed over the semiconductor chip[[:]]~~
- ~~a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern~~ metal pad;
- a molding resin formed over the conductive wiring pattern; and
- ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern[[:]]~~
- a terminal member which is electrically connected to the conductive wiring pattern ~~formed on the molding resin and is connected to the conductive post; and,~~
- wherein
the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion,
~~a connecting portion between the conductive wiring pattern and the conductive~~

~~post~~[[,]]

the connecting portion ~~having~~ has a width that gradually decreases toward the extended portion ~~conductive wiring pattern, and~~

the connecting portion ~~having~~ has a slit to disperse stress ~~[[to be]]~~ applied to the connecting portion.

Claim 2 (Original): A chip-size semiconductor package according to claim 1, wherein the connecting portion is provided with a plurality of slits, which are separated from each other.

Claim 3 (Previously Presented): A chip-size semiconductor package according to claim 2, wherein the slits are rectangular shaped and are arranged to extend radially away from each other.

Claim 4 (Canceled)

Claim 5 (Currently Amended): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

~~a wafer coat formed over the semiconductor chip~~[[;]]

a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is~~

electrically connected to the ~~conductive pattern~~ metal pad;

a molding resin formed over ~~[[on]]~~ the conductive wiring pattern; and

~~a conductive post which is formed in the molding resin and is connected to the~~
~~conductive wiring pattern~~~~[[:]]~~

a terminal member which is electrically connected to the conductive wiring
pattern ~~formed on the molding resin and is connected to the conductive post~~~~[[:]]~~.

wherein

the conductive wiring pattern comprises a terminal portion on which the terminal
member is formed, an extended portion extending from the terminal portion and a
connecting portion arranged between the terminal portion and the extended portion,

~~[[a]]~~ the ~~connecting portion directly between the conductive wiring pattern and~~
~~the conductive post, the connecting portion having~~ has a width that gradually decreases
from a first boundary at the ~~conductive post~~ terminal portion to a second boundary at
the ~~conductive wiring pattern~~~~[[:]]~~ extended portion, and

a dummy pattern arranged adjacent the first and second boundaries and along
sides of the connecting portion, the molding resin also being formed on the dummy
pattern.

Claim 6 (Previously Presented): A chip-size semiconductor package according to claim
5, wherein the dummy pattern is a conductive pattern which is formed during a same
process as the conductive wiring pattern and is arranged parallel to the conductive

wiring pattern.

Claim 7 (Previously Presented): A chip-size semiconductor package according to claim 5, wherein the dummy pattern comprises two parts respectively arranged along both sides of the connecting portion.

Claim 8 (Canceled)

Claim 9 (Currently Amended): A chip-size semiconductor package, comprising:

- a semiconductor chip;
- a metal pad formed on the semiconductor chip;
- ~~a wafer coat formed over the semiconductor chip~~[[:]]
- a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern~~ metal pad;
- a molding resin formed over the conductive wiring pattern; and
- ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[:]]
- a terminal member which is electrically connected to the conductive wiring pattern ~~formed on the molding resin and is connected to the conductive post; and,~~
- wherein
- the conductive wiring pattern comprises a terminal portion on which the terminal

member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and a connecting portion arranged between the terminal portion and the extended portion,

[[a]] ~~the connecting portion directly between the conductive wiring pattern and the conductive post, the connecting portion having~~ has a width that gradually decreases from a first boundary at the ~~conductive post~~ terminal portion to a second boundary at the ~~conductive wiring pattern~~ extended portion, and

~~wherein~~ a dent is formed at and around the connecting portion.

Claim 10 (Previously Presented): A chip-size semiconductor package according to claim 9, wherein the dent is square shaped.

Claim 11 (Canceled)

Claim 12 (Currently Amended): A chip-size semiconductor package, comprising:

- a semiconductor chip;
- a metal pad formed on the semiconductor chip;
- ~~a wafer coat formed over the semiconductor chip[[:]]~~
- a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is electrically connected to the~~ conductive wiring pattern metal pad;
- a molding resin formed over the conductive wiring pattern; and

~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[:]]

a terminal member which is electrically connected to the conductive wiring pattern ~~formed on the molding resin and is connected to the conductive post; and,~~
wherein

the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion,

[[a]] the connecting portion ~~directly between the conductive wiring pattern and the conductive post, the connecting portion having~~ has a width that gradually decreases from a first boundary at the ~~conductive post~~ terminal portion to a second boundary at the ~~conductive wiring pattern~~ extended portion, and

the connecting portion ~~having~~ has a first region extending outwardly from the ~~conductive post~~ terminal portion and a second region extending in a perpendicular direction from the first region, the second region extending from the connecting portion.

Claim 13 (Previously Presented): A chip-size semiconductor package according to claim 12, further comprising a plurality of projecting parts each of which extends in the perpendicular direction from the conductive wiring pattern.

Claim 14 (Previously Presented): A chip-size semiconductor package according to

claim 13, wherein the second region extends from both sides of the first region.

Claims 15-17 (Canceled)

Claim 18 (New): A chip-size semiconductor package according to claim 1, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 19 (New): A chip-size semiconductor package according to claim 5, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 20 (New): A chip-size semiconductor package according to claim 9, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 21 (New): A chip-size semiconductor package according to claim 12, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 22 (New): A chip-size semiconductor package according to claim 1, wherein the

terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.

Claim 23 (New): A chip-size semiconductor package according to claim 5, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.

Claim 24 (New): A chip-size semiconductor package according to claim 9, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.

Claim 25 (New): A chip-size semiconductor package according to claim 12, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.